

REMARKS

The Office Action mailed on June 26, 2003 subjected pending claims 14 – 31 to a two-way requirement for restriction requiring the Applicant to make an election under 35 U.S.C. § 121 of one of the following inventions:

Group I: Claims 14 – 21 and 27 – 30, drawn to a method of making plural semiconductor device mounting regions; and

Group II: Claims 22 – 26 and 31, drawn to plural semiconductor device mounting regions.

The Office Action notes and concedes that “the process as claimed can be used to make other and materially different product.” Specifically, the Office Action notes that “the product as claimed can be made by another and materially different process, such as: the openings in the insulating support member could be made by masking the terminal regions, then forming insulation in the areas in between.” The Office Action’s rationale, however, does not present a serious burden because a proper search should uncover both the process where the insulating support member is formed before the openings are formed and the process where the terminal regions are masked prior to the formation of the insulating layer.

Applicant, as required under 35 U.S.C. § 121, provisionally elects Group II (Claims 22 – 26 and 31) and respectfully traverse the requirement for restriction. It should be noted that as a practical matter examination of claims 14 – 31, covering Group I and II does not require separate or burdensome searches.

Applicants have traversed the requirement for restriction and hereby request that either the requirement for restriction be withdrawn in view of the reasons recited herein or be made final.

Claim 31 has been amended to explicitly incorporate all the limitations of non-elected claim 27 and retains the full scope and breadth of originally filed claim 31.

REMARKS CONCERNING REVISED FIGURES

Appendix A includes revised drawing sheets 1, 3 – 7, 9 – 13, 16 – 21, and 23 – 24. The revised drawings correct inconsistent hatching patterns in the originally filed drawings. For example, the hatching pattern for LSI chip 3 in Figs. 1a-c is

different than the hatching pattern in Figs. 1d-f. Similar hatching inconsistencies are corrected in the other revised drawing sheets.

In the originally filed Fig. 11d, wire bond 100 is shown penetrating into wire 2 and is corrected to show termination of the wire bond 100 at the surface of wire 2 in the revised drawing. The revised Fig. 11d is consistent with the terminations shown in Figs. 11e-g and the left portion of Fig. 11d. Therefore no new matter has been added.

In originally filed Fig. 17, the hatching pattern for adhesive 36 is the same as the hatching pattern for resinous sealing material 41 although both structures are distinct and different from each other. The revised Fig. 17 corrects this error by employing a different hatching pattern for the resinous sealing material 41 in Figs. 17f-g. Therefore no new matter has been added by the revision.

An early allowance of the application is earnestly requested. The Examiner is invited to contact Steven Fukuda at 212.790.6524 with any questions concerning the foregoing.

No fee is believed to be due for this submission. Should any fees be required, however, please charge such fees to Pennie & Edmonds Deposit Account No. 16-1150.

Respectfully submitted,

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